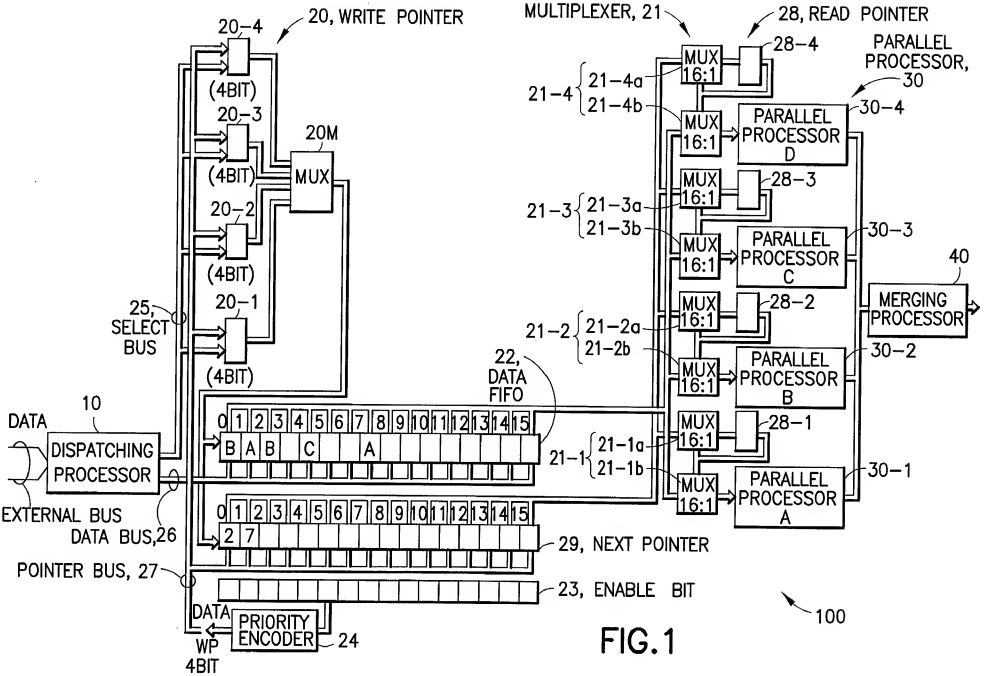
20-4
20, WRITE POINTER
(4BIT)
20-3
(4BIT)
20M
MUX
20-2
(4BIT)
20-1
(4BIT)
25, SELECT BUS
10
DATA
DISPATCHING PROCESSOR
EXTERNAL BUS
DATA BUS, 26
POINTER BUS, 27
22, DATA FIFO
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
B A B C A
2 7
29, NEXT POINTER
23, ENABLE BIT
DATA
PRIORITY ENCODER
24
WP 4BIT
MULTIPLEXER, 21
28, READ POINTER
28-4
PARALLEL PROCESSOR, 30
21-4
21-4a
21-4b
MUX 16:1
PARALLEL PROCESSOR D
30-4
21-3
21-3a
21-3b
28-3
PARALLEL PROCESSOR C
30-3
40
MERGING PROCESSOR
21-2
21-2a
21-2b
28-2
PARALLEL PROCESSOR B
30-2
21-1
21-1a
21-1b
28-1
PARALLEL PROCESSOR A
30-1
100

FIG.1

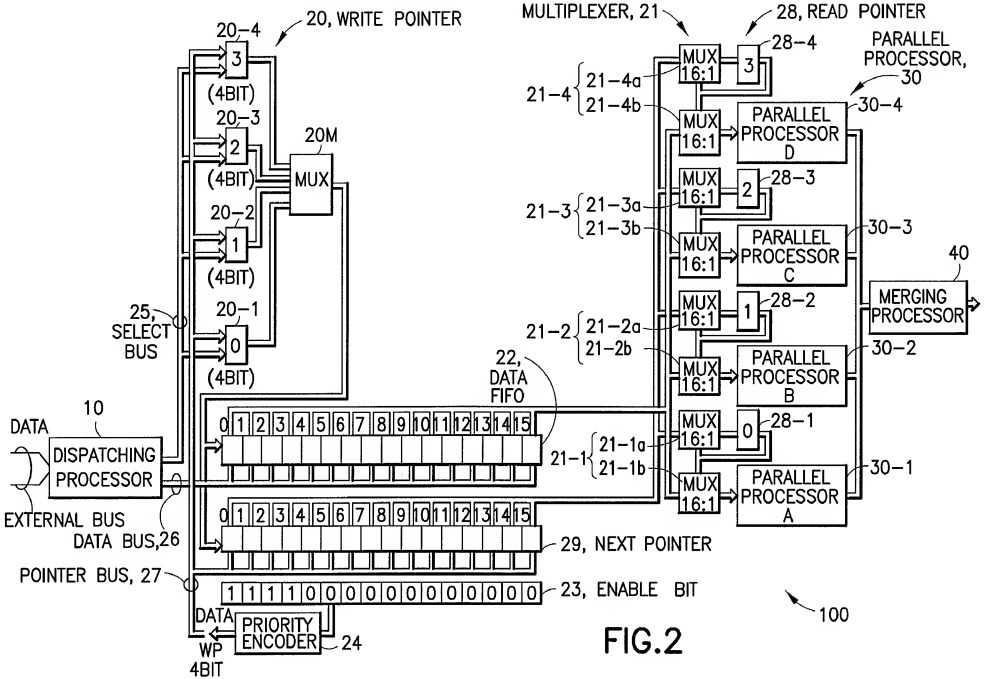
20, WRITE POINTER
MULTIPLEXER, 21
28, READ POINTER
PARALLEL PROCESSOR, 30
20-4
20-3
20-2
20-1
(4BIT)
20M
MUX
25, SELECT BUS
22, DATA FIFO
10
DATA
DISPATCHING PROCESSOR
EXTERNAL BUS
DATA BUS, 26
POINTER BUS, 27
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
29, NEXT POINTER
1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
23, ENABLE BIT
DATA
PRIORITY ENCODER
24
WP 4BIT
100
21-4
21-4a
21-4b
21-3
21-3a
21-3b
21-2
21-2a
21-2b
21-1
21-1a
21-1b
MUX 16:1
28-4
28-3
28-2
28-1
PARALLEL PROCESSOR D
PARALLEL PROCESSOR C
PARALLEL PROCESSOR B
PARALLEL PROCESSOR A
30-4
30-3
30-2
30-1
40
MERGING PROCESSOR

FIG.2

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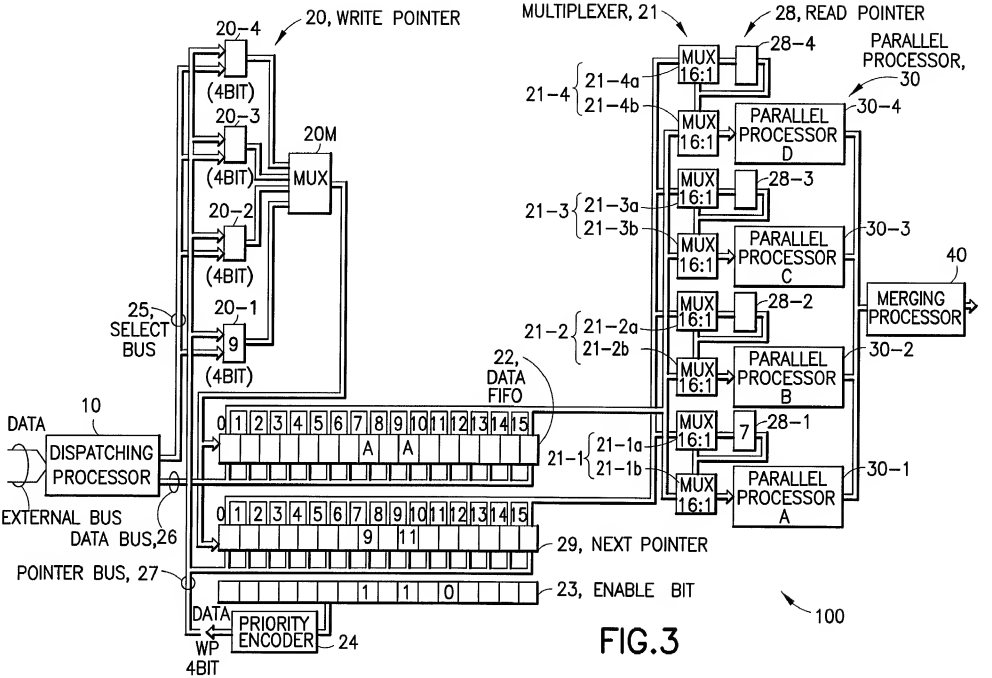

FIG.3

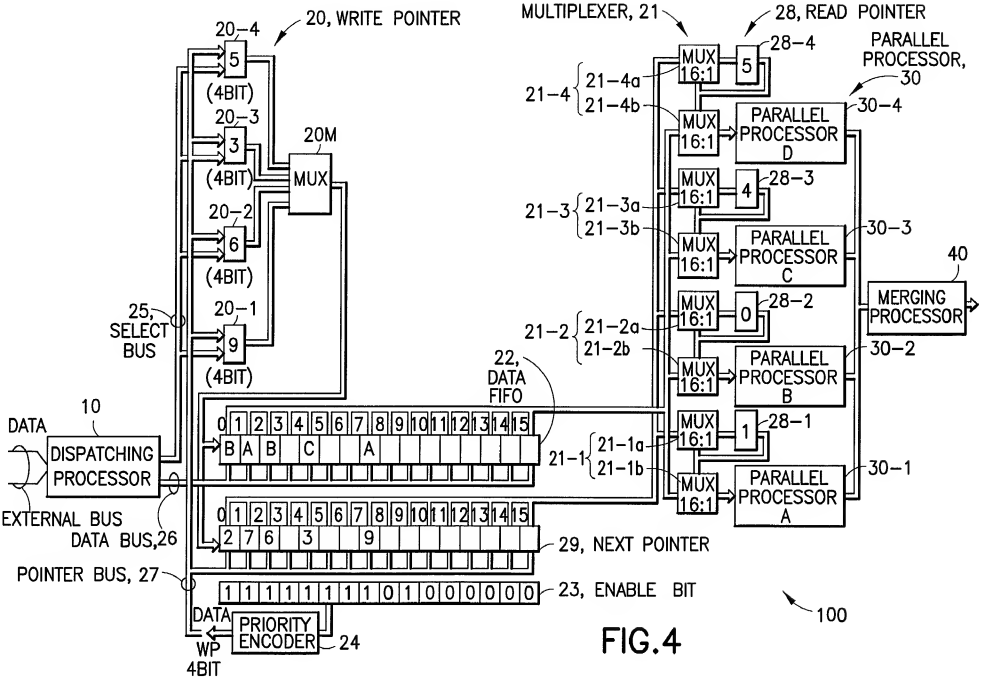
20, WRITE POINTER
MULTIPLEXER, 21
28, READ POINTER
PARALLEL PROCESSOR, 30
20-4
5
(4BIT)
20-3
3
(4BIT)
20-2
6
(4BIT)
20-1
9
(4BIT)
20M
MUX
25, SELECT BUS
22, DATA FIFO
10
DATA
DISPATCHING PROCESSOR
EXTERNAL BUS
DATA BUS, 26
POINTER BUS, 27
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
B A B C A
2 7 6 3 9
29, NEXT POINTER
1 1 1 1 1 1 1 1 0 1 0 0 0 0 0 0
23, ENABLE BIT
DATA
PRIORITY ENCODER
24
WP 4BIT
100
21-4
21-4a
21-4b
21-3
21-3a
21-3b
21-2
21-2a
21-2b
21-1
21-1a
21-1b
MUX 16:1
28-4
28-3
28-2
28-1
PARALLEL PROCESSOR D
PARALLEL PROCESSOR C
PARALLEL PROCESSOR B
PARALLEL PROCESSOR A
30-4
30-3
30-2
30-1
40
MERGING PROCESSOR

FIG.4

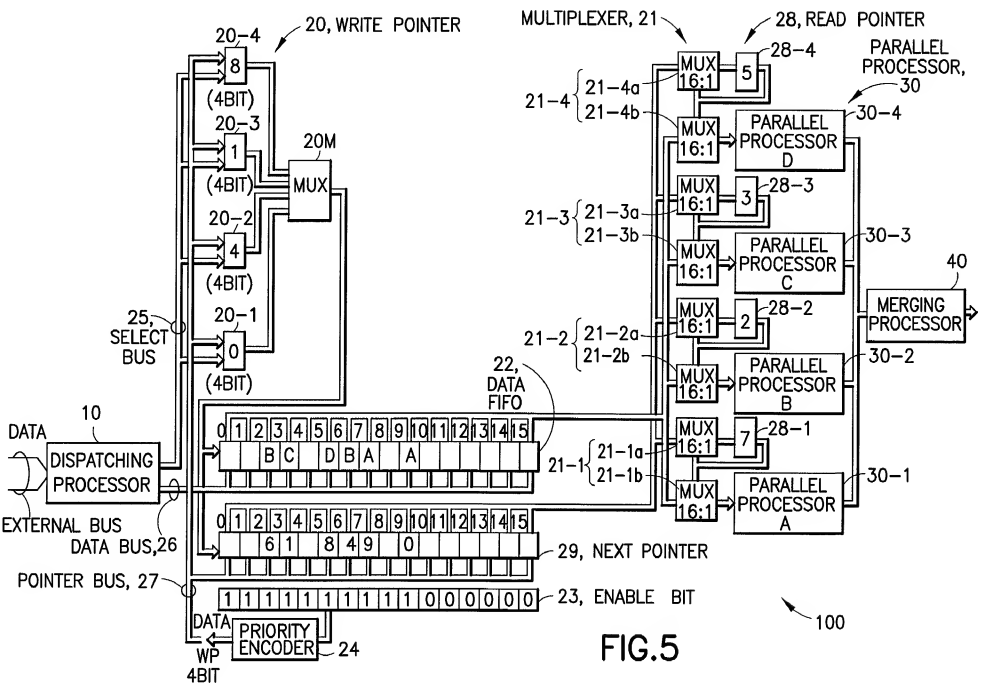
20-4
20, WRITE POINTER
8
(4BIT)
20-3
1
(4BIT)
20M
MUX
20-2
4
(4BIT)
20-1
0
(4BIT)
25, SELECT BUS
10
DATA
DISPATCHING PROCESSOR
EXTERNAL BUS
DATA BUS, 26
POINTER BUS, 27
22, DATA FIFO
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
B C D B A A
21-1
21-1a
21-1b
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
6 1 8 4 9 0
29, NEXT POINTER
1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0
23, ENABLE BIT
DATA
PRIORITY ENCODER
24
WP 4BIT
MULTIPLEXER, 21
28, READ POINTER
PARALLEL PROCESSOR, 30
21-4
21-4a
21-4b
MUX 16:1
5
28-4
PARALLEL PROCESSOR D
30-4
21-3
21-3a
21-3b
3
28-3
PARALLEL PROCESSOR C
30-3
21-2
21-2a
21-2b
2
28-2
PARALLEL PROCESSOR B
30-2
7
28-1
PARALLEL PROCESSOR A
30-1
40
MERGING PROCESSOR
100

FIG.5

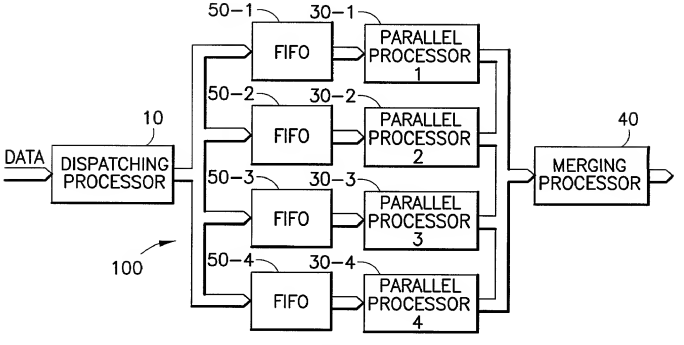

FIG.6

	CASE(a)	CASE(b)	CASE(c)
PARALLEL PROCESSOR 1	1	2	2
PARALLEL PROCESSOR 2	3	1	8
PARALLEL PROCESSOR 3	2	5	1
PARALLEL PROCESSOR 4	1	1	3

FIG.7

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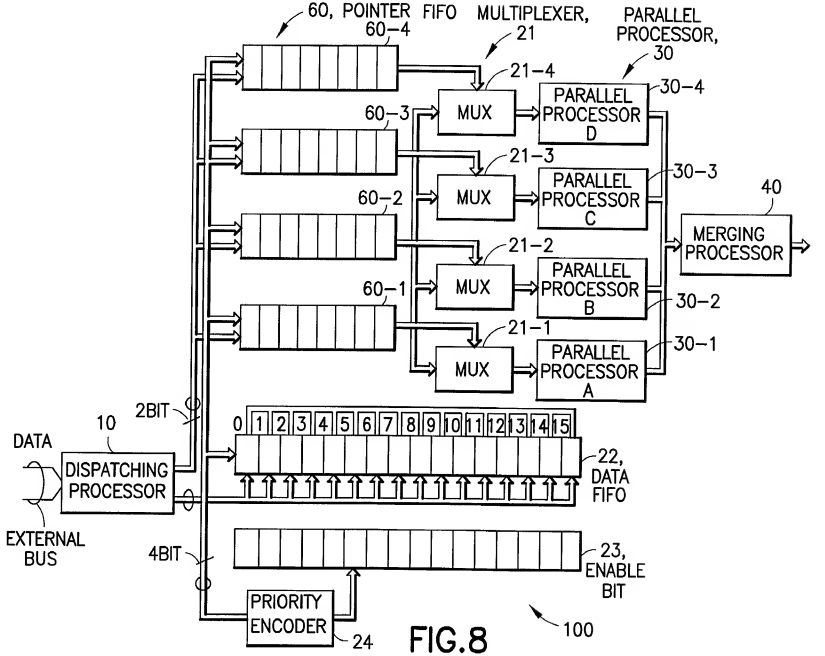

FIG.8